RESIDENTIAL DC MICROGRID PROTECTION METHODS

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TALLINN UNIVERSITY OF TECHNOLOGY

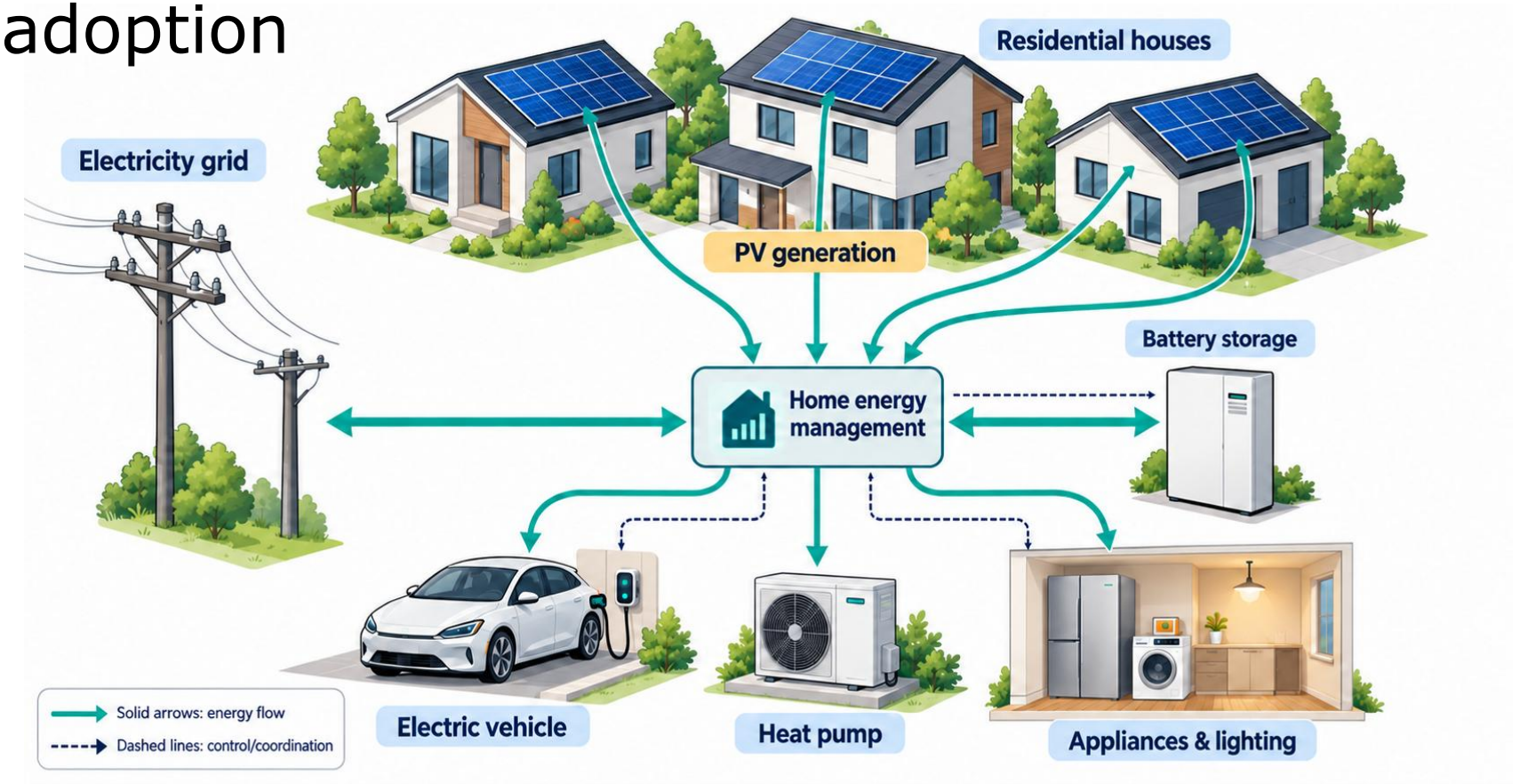
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INTRODUCTION



GLOBAL ELECTRIFICATION TRENDS

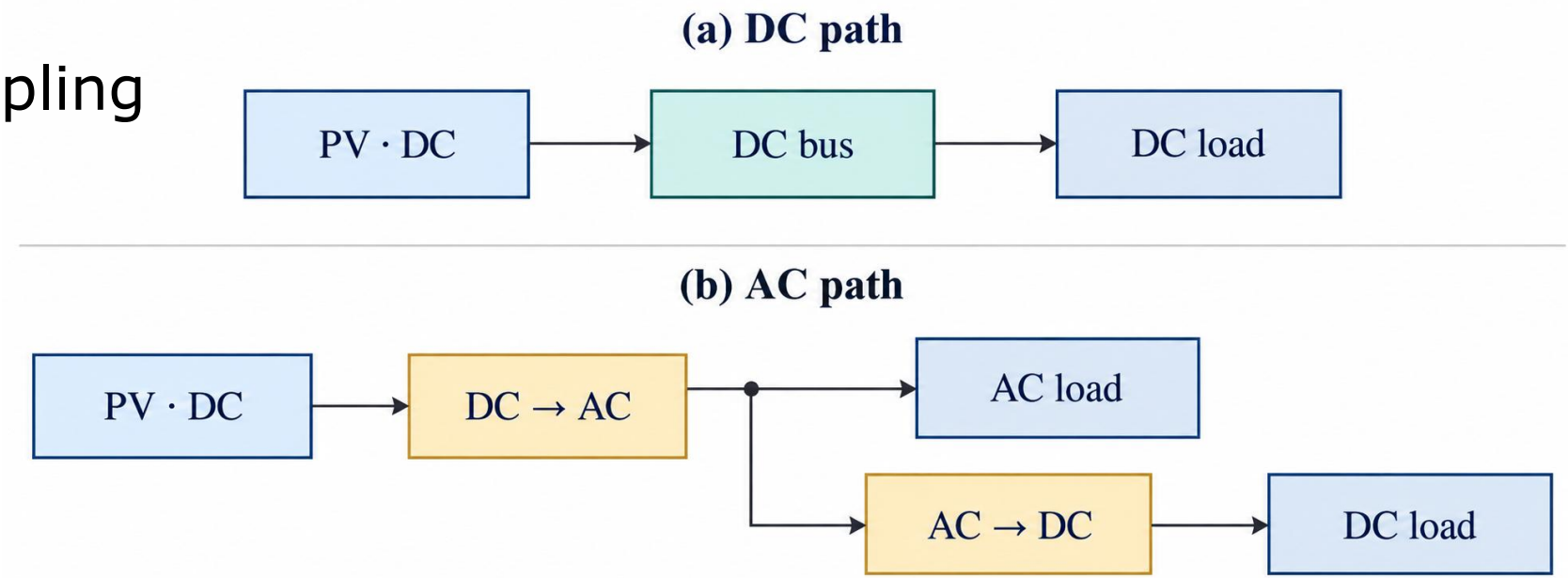
- Solar PV growth
- Battery storage adoption
- Electric vehicles
- DC-native loads



WHY DC IN RESIDENTIAL BUILDINGS?

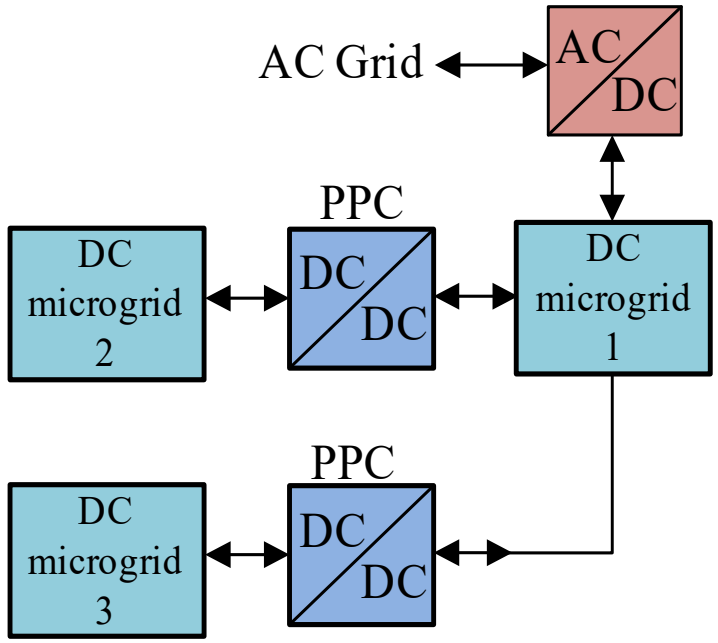
Advantages:

- Reduced number of conversion stages
- Higher efficiency
- Better renewable integration
- Easier battery coupling
- Compatibility with electronic loads

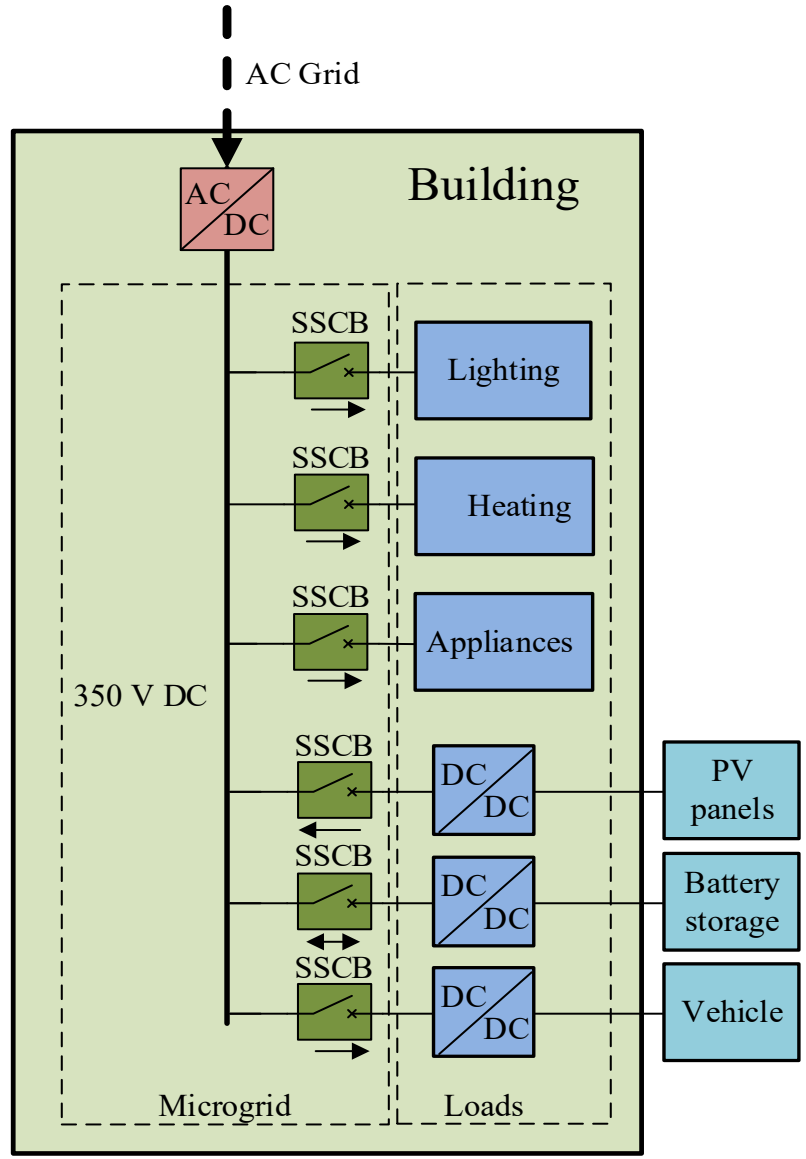


WHAT IS A RESIDENTIAL DC MICROGRID?

- Electrical network of limited dimensions (and/or power), where direct current is used.



DC microgrid connection to other grids

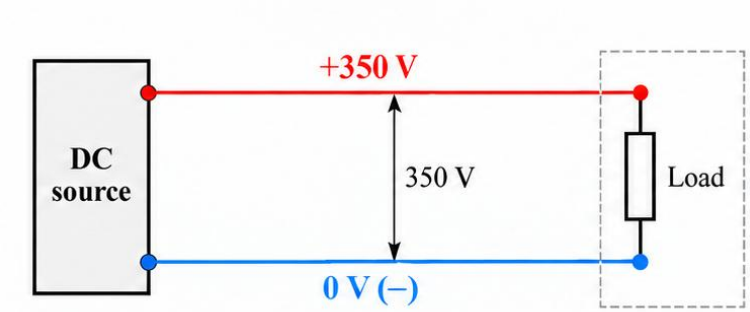


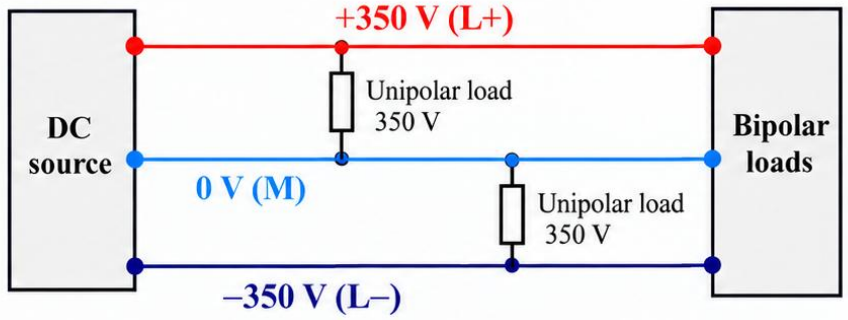
Typical DC microgrid

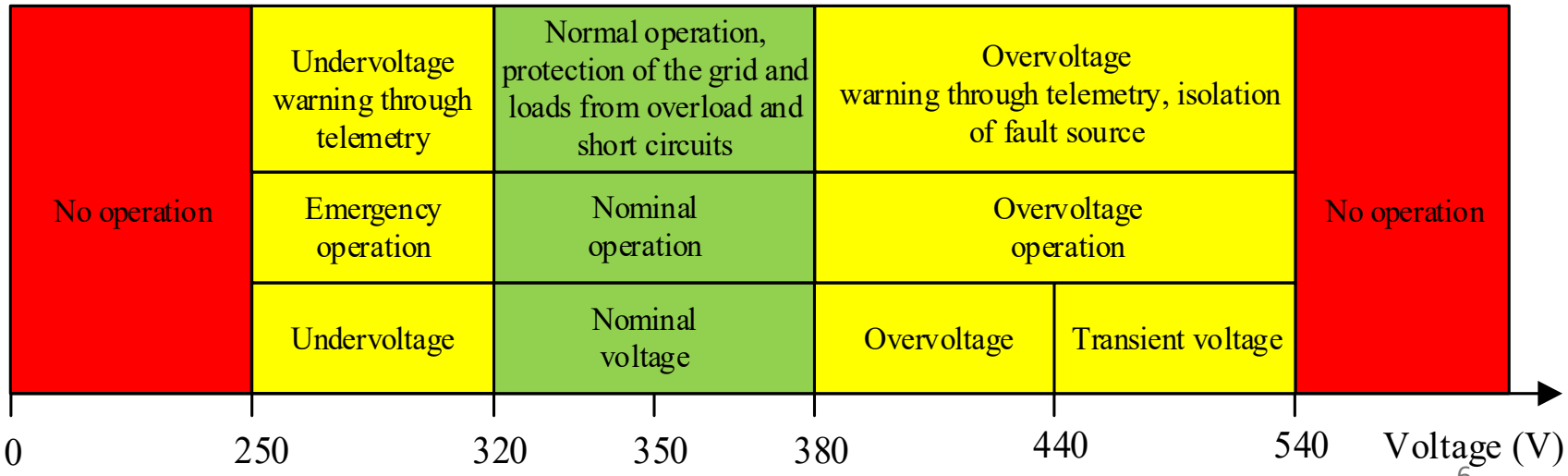
TYPICAL VOLTAGE LEVELS

Residential standards:

- 12 V DC
- 48 V DC
- **350 V DC**
- 700 V DC



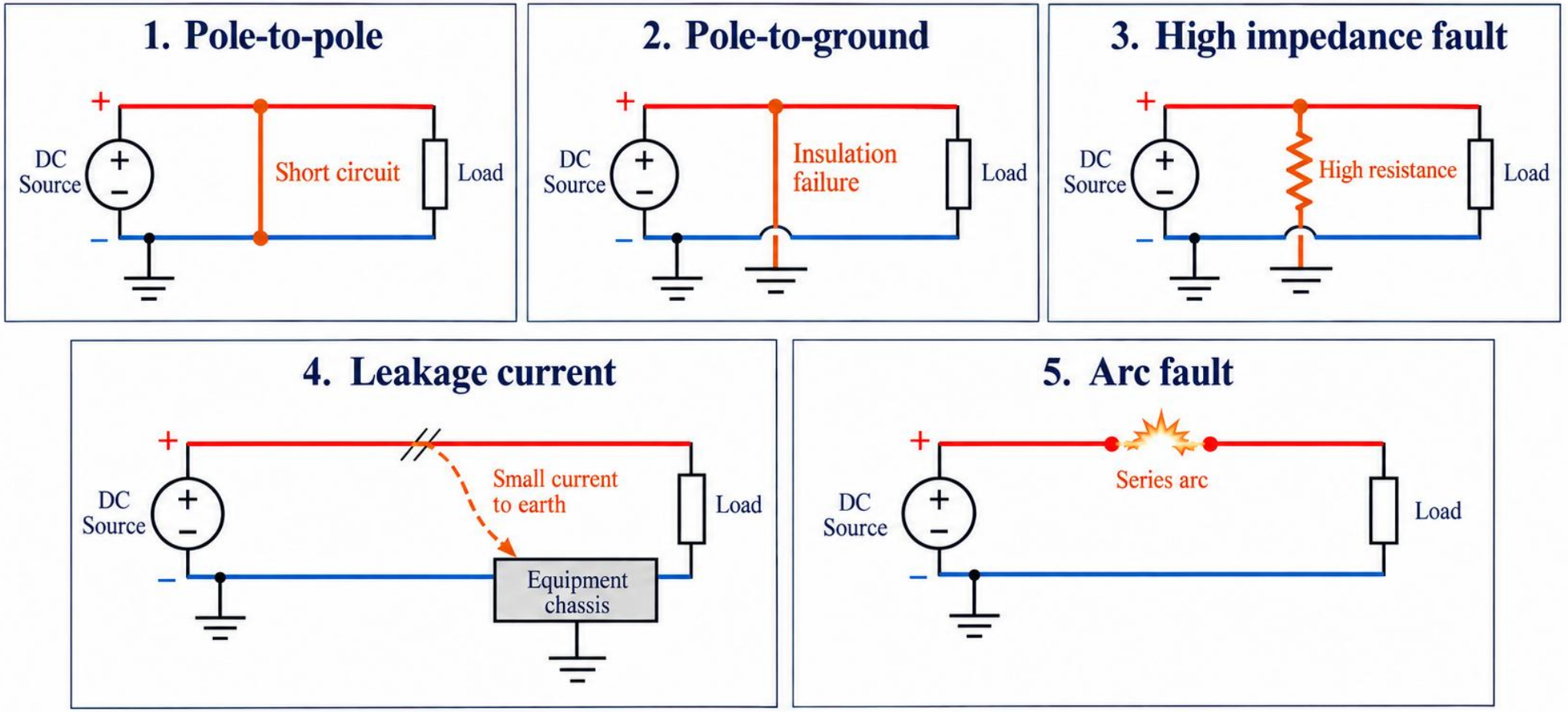




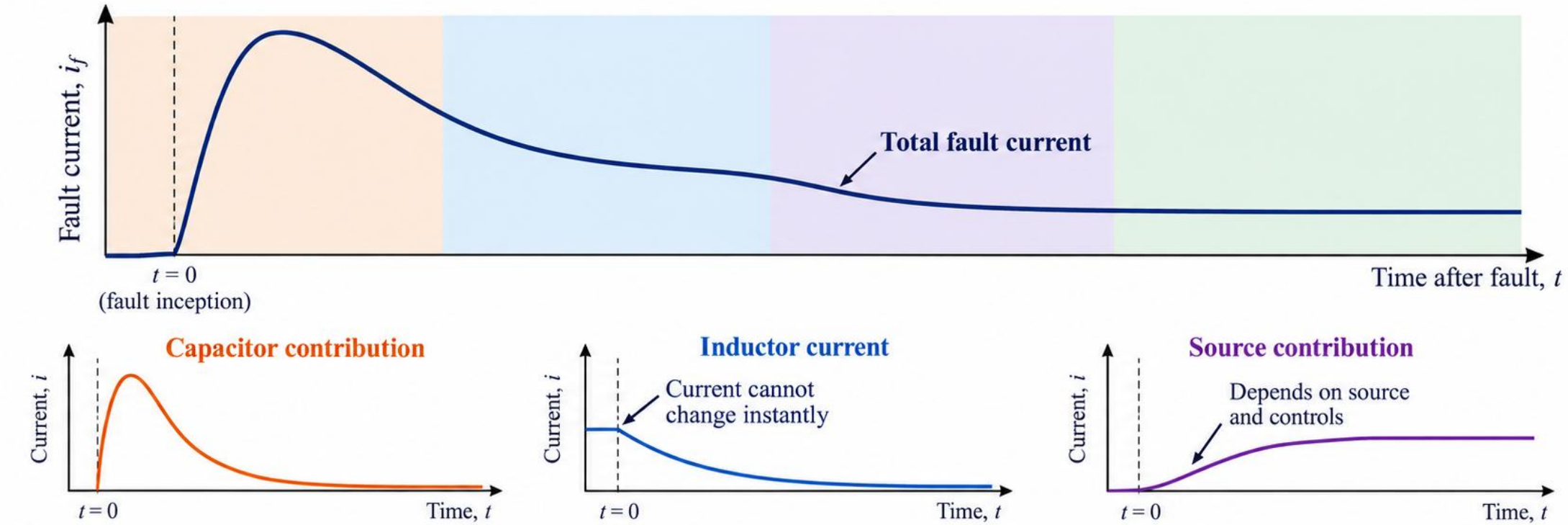
FAULTS IN DC MICROGRIDS



UNDERSTANDING DC FAULTS



FAULT CURRENT EVOLUTION



1. Capacitor discharge

Stored electric energy drives an early current surge

2. Inductor response

Inductance limits *di/dt* and releases stored energy

3. Source contribution

Source and converter controls shape the current

4. Steady-state fault

Sustained current if the fault remains uncleared

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PROTECTION CHALLENGES



WHY DC FAULTS ARE DIFFICULT

Key challenges:

- No natural current zero crossing
- Not all leakage current measurement methods work with DC

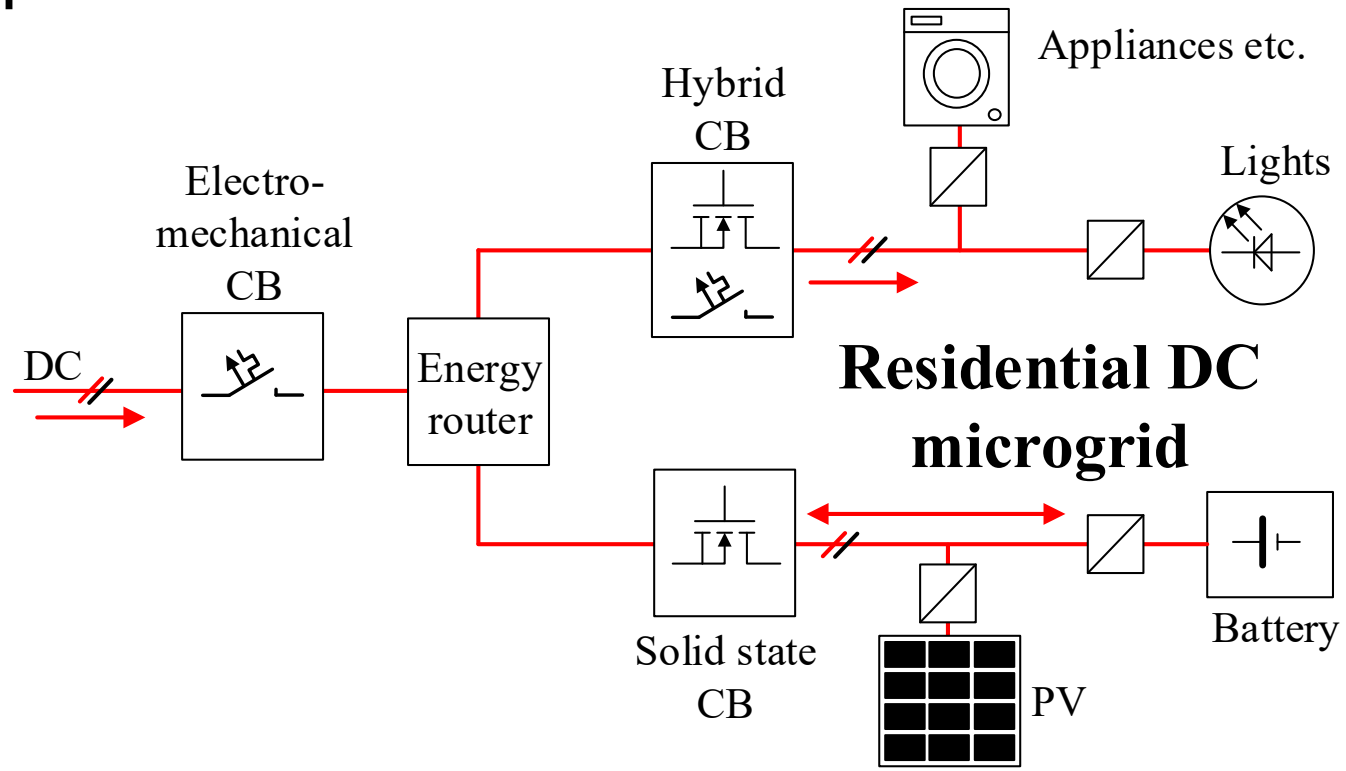
Consequences:

- Sustained arcs
- Thermal stress
- Equipment damage
- Risk of electrocution

PROTECTION COORDINATION ISSUES IN MICROGRIDS

Challenges:

- Bidirectional power flow
- Distributed generation



REQUIREMENTS FOR PROTECTION DEVICES



REQUIREMENTS (STANDARDS/INITIATIVES)

- Low-voltage DC standards
- **IEC 60364-8-82** (residential/prosumer DC installation)
- **IEEE 2030.10** (DC microgrids)
- **EN IEC 60898-3** (DC breakers for residential use)
- **EN IEC 60947-2** (AC and DC breakers for industrial use)

- DC initiatives
- **Current/OS** (nonprofit, open partnership advancing hybrid AC/DC power distribution)
- **Open Direct Current Alliance (ODCA)** (low-voltage DC grids for factories, buildings, campuses)
- **EMerge Alliance** (hybrid AC/DC buildings, DC Microgrids)
- **IEC SyC LVDC** (IEC systems committee dedicated to Low Voltage Direct Current)
- **i³DC/TalTech** (residential DC)

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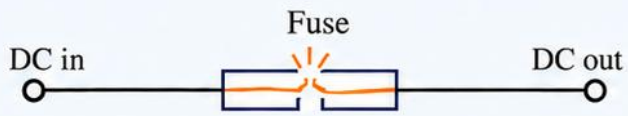
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DC PROTECTION TECHNOLOGIES



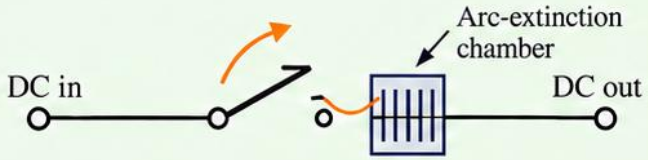
OVERVIEW OF DC PROTECTION METHODS

1 Fuses



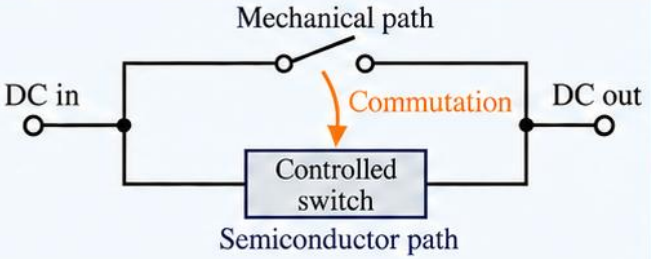
Melting element interrupts overcurrent
Replacement required after operation

2 Mechanical breakers



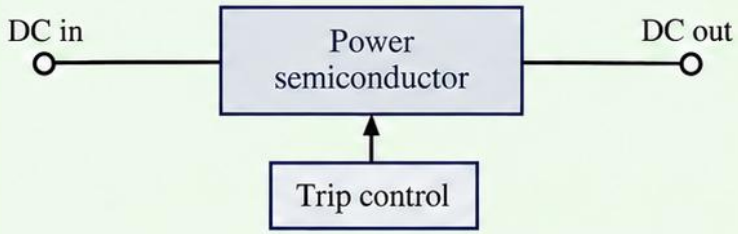
A bimetallic or electromagnetic mechanism opens the contacts in the event of overcurrent.
DC arc must be extinguished

3 Hybrid breakers



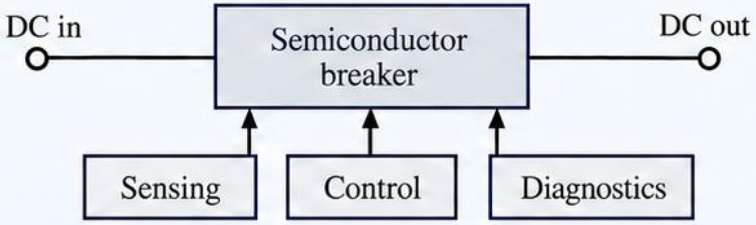
Mechanical and semiconductor paths cooperate
Low conduction loss with fast interruption

4 Solid-state breakers



Electronic switching interrupts fault current
Very fast operation; conduction losses

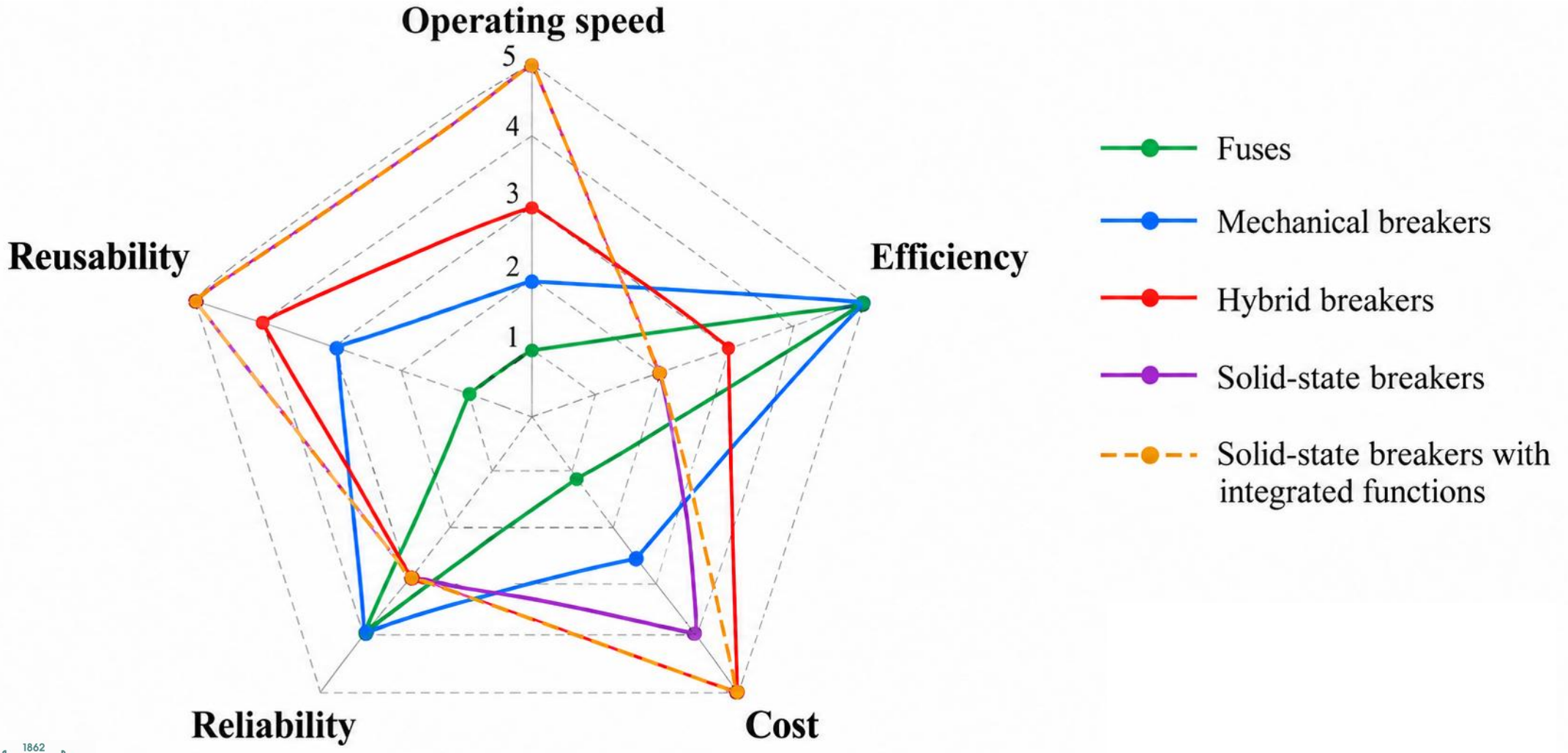
5 Solid-state breakers with integrated functions



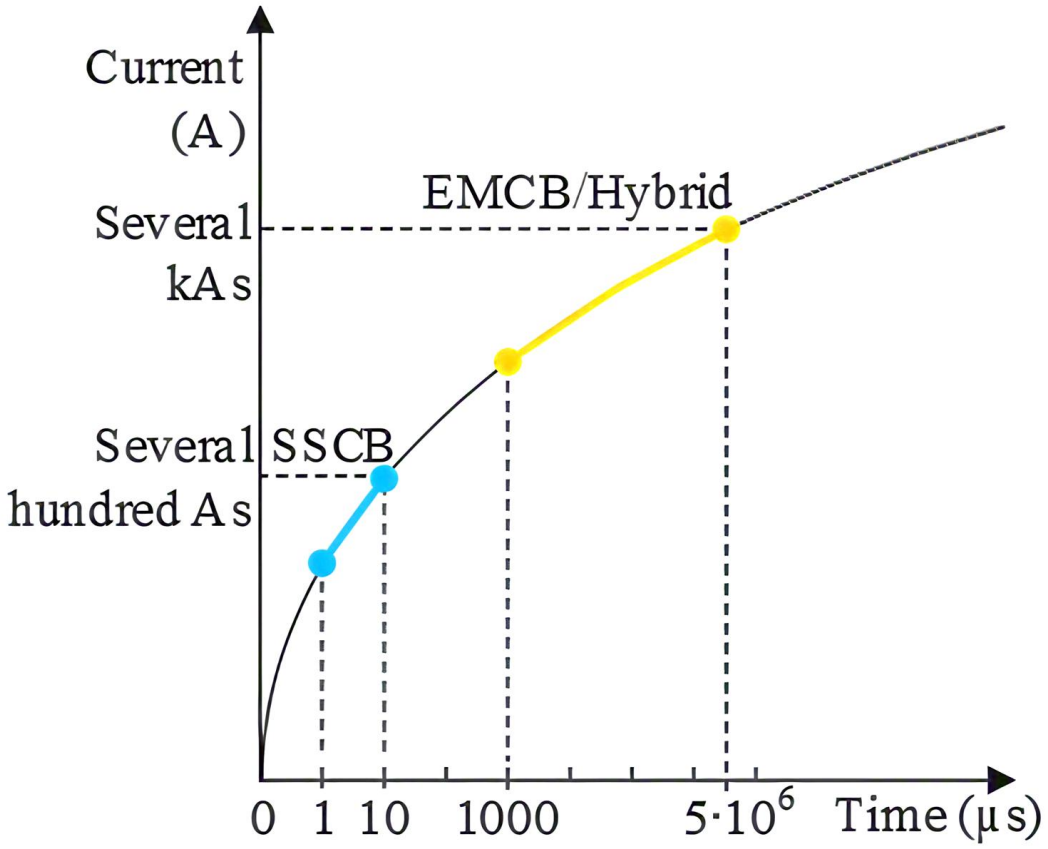
Protection combined with electronic functions
May include residual current and arc sensing

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COMPARATIVE PERFORMANCE

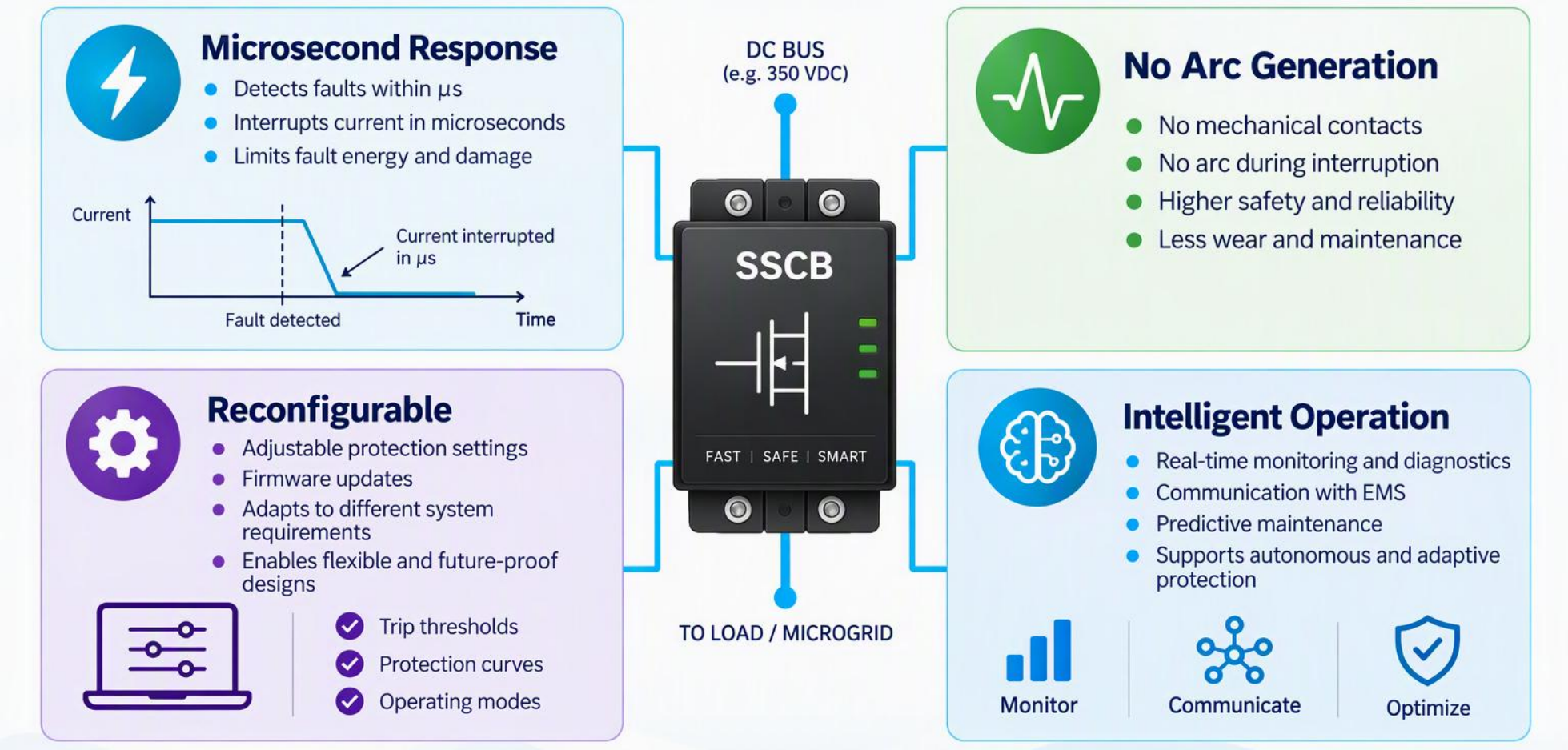


COMPARATIVE PERFORMANCE



Protection method	Operating speed during short circuit	Current-breaking capability
Fuses	Strongly current-dependent: milliseconds to seconds.	Tens of kiloamperes.
Mechanical breakers	Typically tens of milliseconds	Tens of kiloamperes.
Hybrid breakers	Typically 1–5 ms	Tens of kiloamperes.
Solid-state breakers	Microseconds to hundreds of microseconds.	Hundreds of amperes

WHY SSCBS (SOLID STATE CIRCUIT BREAKERS) ARE ATTRACTIVE



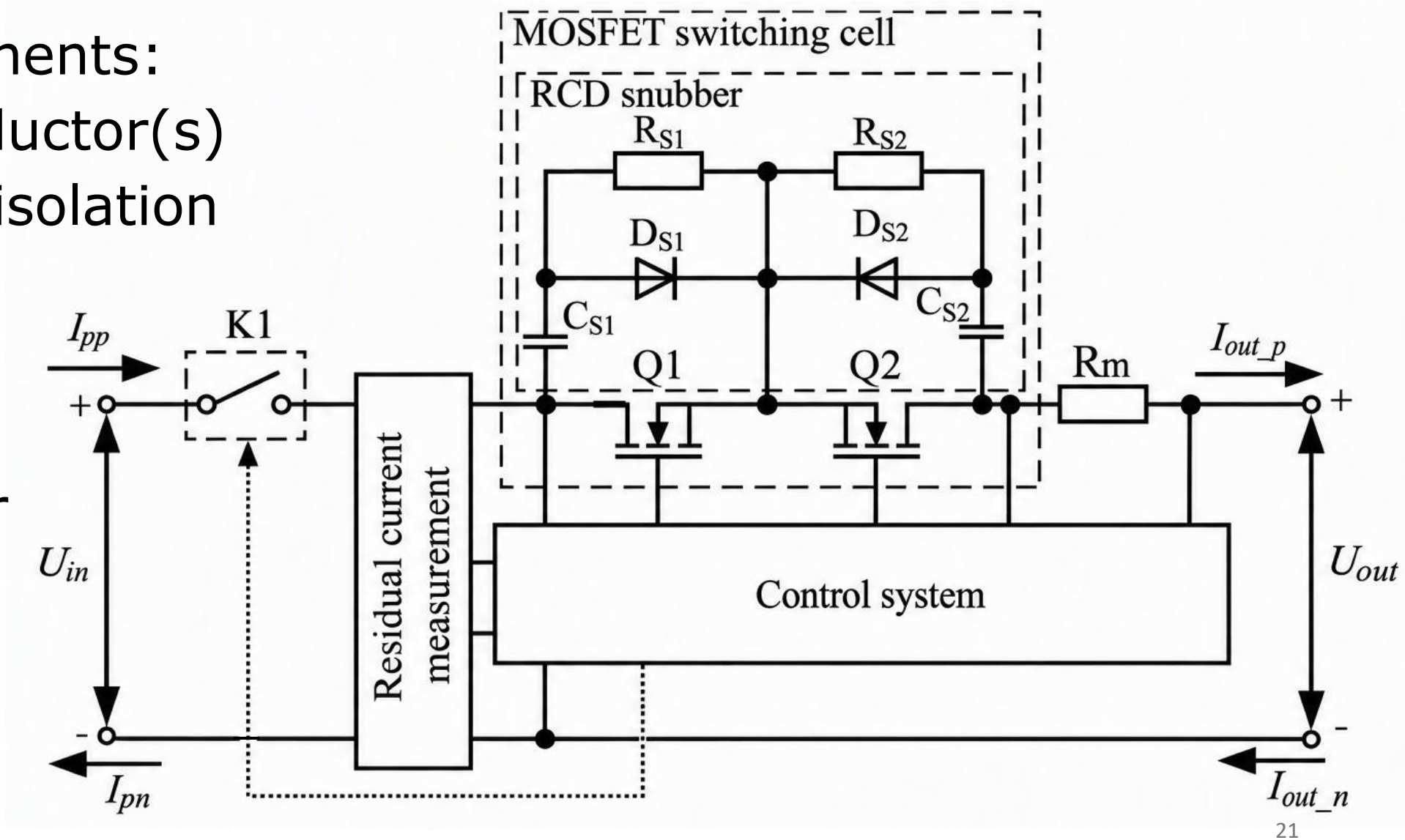
SOLID-STATE CIRCUIT BREAKER DESIGN



SSCB OPERATING PRINCIPLE

Key components:

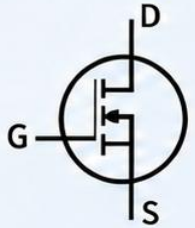
- Semiconductor(s)
- Galvanic isolation
- Snubbers
- Drivers
- Sensors
- Controller



DEVICE TECHNOLOGIES

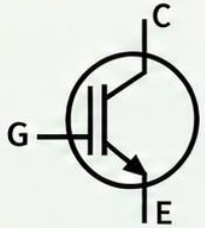
Si MOSFET

Mature and cost-effective
for low-medium voltage DC systems



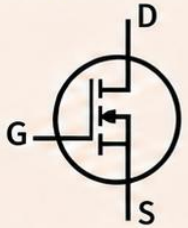
IGBT

High voltage capability
for higher power applications



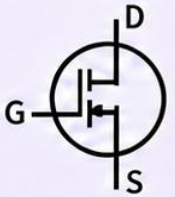
SiC MOSFET

Wide-bandgap performance
for next-generation SSCBs



GaN HEMT

Ultra-fast switching
for low-medium voltage,
high-frequency applications

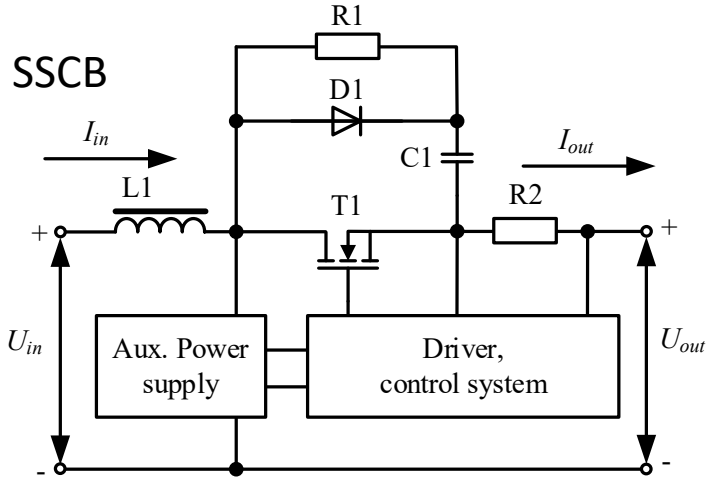


Parameter	Si MOSFET	IGBT	SiC MOSFET	GaN HEMT
Voltage rating (typical)	12 – 1000 V	300 – 1700 V	650 – 3300 V	40 – 650 V
Current capability	Up to few hundred A	Hundreds of A to kA	Tens to hundreds of A	Tens of A (increasing)
Switching speed	Fast (tens of ns)	Moderate (100 ns – µs)	Very fast (tens of ns)	Ultra-fast (few ns)
Conduction loss ($R_{DS(on)}$ / $V_{CE(sat)}$)	Low (mΩ range)	Moderate (1 – 3 V)	Very low (mΩ range)	Very low (mΩ range)
Efficiency	High	Medium	Very high	Very high
Thermal performance	Good	Good	Excellent (high T_j)	Good (high T_j)
Cost	Low	Low – medium	Medium – high	High (but decreasing)
Technology maturity	Very mature	Mature	Rapidly growing	Growing
Typical applications in SSCBs	Low-voltage residential DC	Higher-voltage residential DC	Medium-high voltage SSCBs	Low-medium voltage, high-frequency SSCBs

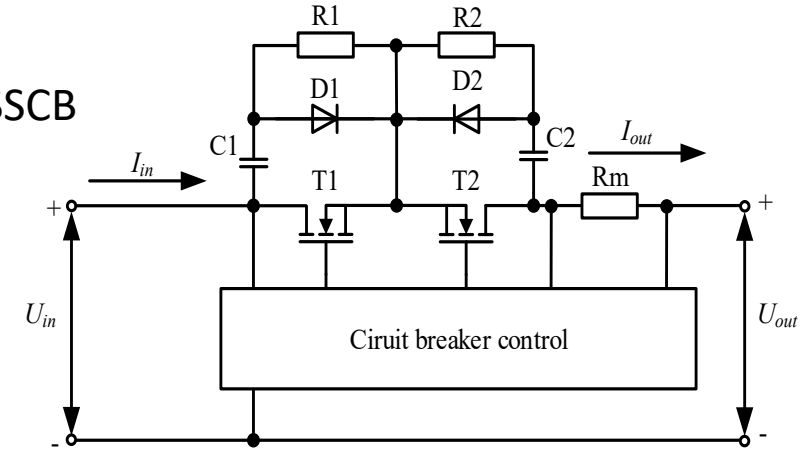
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SSCB TOPOLOGIES

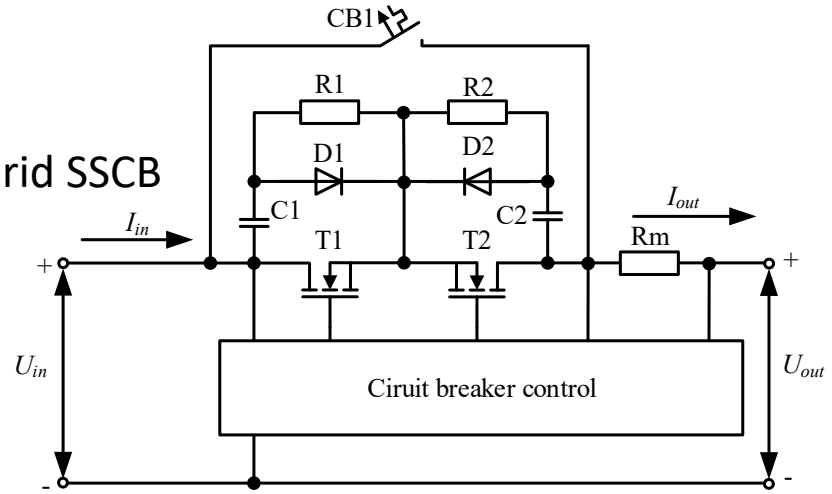
(a) Unidirectional SSCB



(b) Bidirectional SSCB



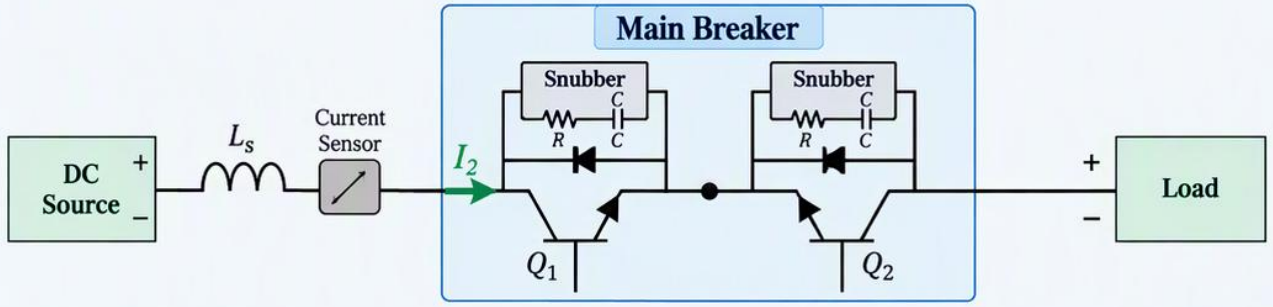
(c) Hybrid SSCB



THERMAL DESIGN AND LOSS ESTIMATION

1. Conduction Design (Electrical)

SSCB Main Breaker Topology (Back-to-Back MOSFETs)



MOSFET Conduction Loss (per device)

$$P_{cond} = I_{rms}^2 \cdot R_{DS(on)}$$

I_{rms} : RMS current through MOSFET (A)
$R_{DS(on)}$: On-state resistance (Ω, at T_j)
P_{cond} : Conduction loss per MOSFET (W)

Total Conduction Loss (SSCB)

$$P_{cond,total} = 2 \cdot I_{rms}^2 \cdot R_{DS(on)}$$

Notes:

- Two MOSFETs conduct in normal operation
- $R_{DS(on)}$ increases with temperature

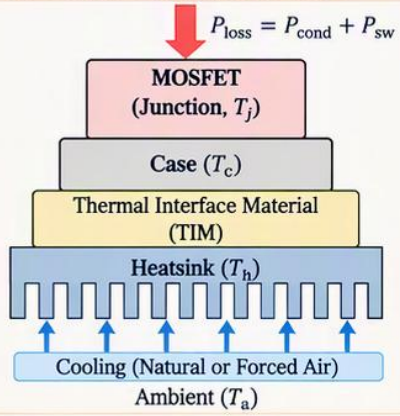
Temperature Dependence

$$R_{DS(on)}(T_j) = R_{DS(on),25°C}\,(1 + \alpha \Delta T)$$

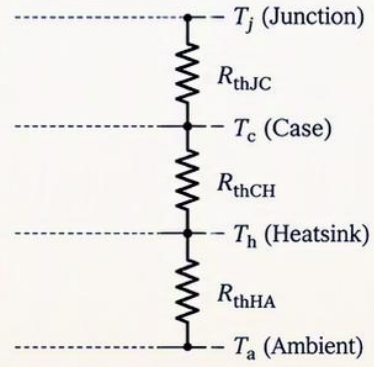
$R_{DS(on),25°C}$: On-state resistance at 25°C
α : Temperature coefficient (1/°C)
ΔT : $T_j - 25°C$

2. Thermal Design (Heat Flow and Temperature Rise)

Thermal Path of a MOSFET in SSCB



Equivalent Thermal Resistance Network



Junction Temperature Calculation

$$T_j = T_a + P_{total}\,(R_{thJC} + R_{thCH} + R_{thHA})$$

T_j : Junction temperature (°C)
T_a : Ambient temperature (°C)
P_{total} : Total power loss per MOSFET (W)
R_{thJC} : Junction-to-case thermal resistance (°C/W)
R_{thCH} : Case-to-heatsink thermal resistance (°C/W)
R_{thHA} : Heatsink-to-ambient thermal resistance (°C/W)

Design Considerations

- Ensure $T_j < T_{j,max}$ (e.g., 150 °C)
- Use low $R_{DS(on)}$ MOSFETs to reduce P_{cond}
- Select suitable heatsink (low R_{thHA})
- Use high-performance TIM (low R_{thCH})
- Consider forced-air or liquid cooling for high power applications
- Include temperature sensing and derating
- Verify thermal performance under fault and steady-state conditions

3. Design Workflow

1. Define Requirements
- Rated current (I_{DC})
- Rated voltage (V_{DC})
- Ambient temperature (T_a)
- Switching duty / fault handling

2. Select MOSFET
- Voltage rating (V_{DS})
- Low $R_{DS(on)}$
- Current rating (I_D)
- Thermal specifications (R_{thJC}, $T_{j,max}$)

3. Calculate Losses
- Conduction loss ($I_{rms}^2 \cdot R_{DS(on)}$)
- Switching loss (P_{sw})
- Total loss per device (P_{total})

4. Thermal Design
- Determine thermal resistances
- Select heatsink and cooling method
- Calculate junction temperature (T_j)
- Check thermal margins

5. Validate and Iterate
- Verify electrical and thermal performance
- Evaluate under fault conditions
- Optimize for size, cost and efficiency

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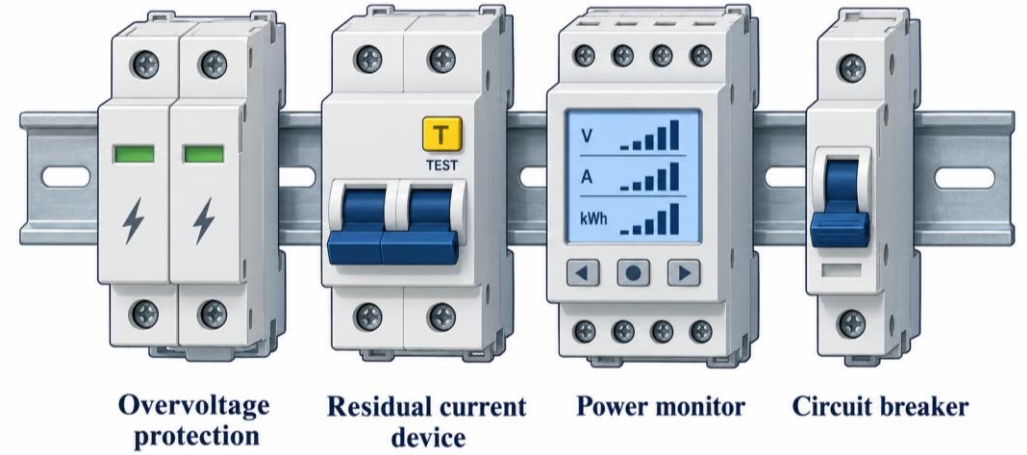
INTEGRATED PROTECTION METHODS

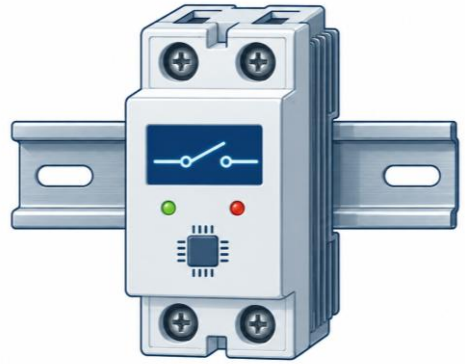


CONCEPT OF INTEGRATED PROTECTION

Traditional approach:
External device(s) + breaker

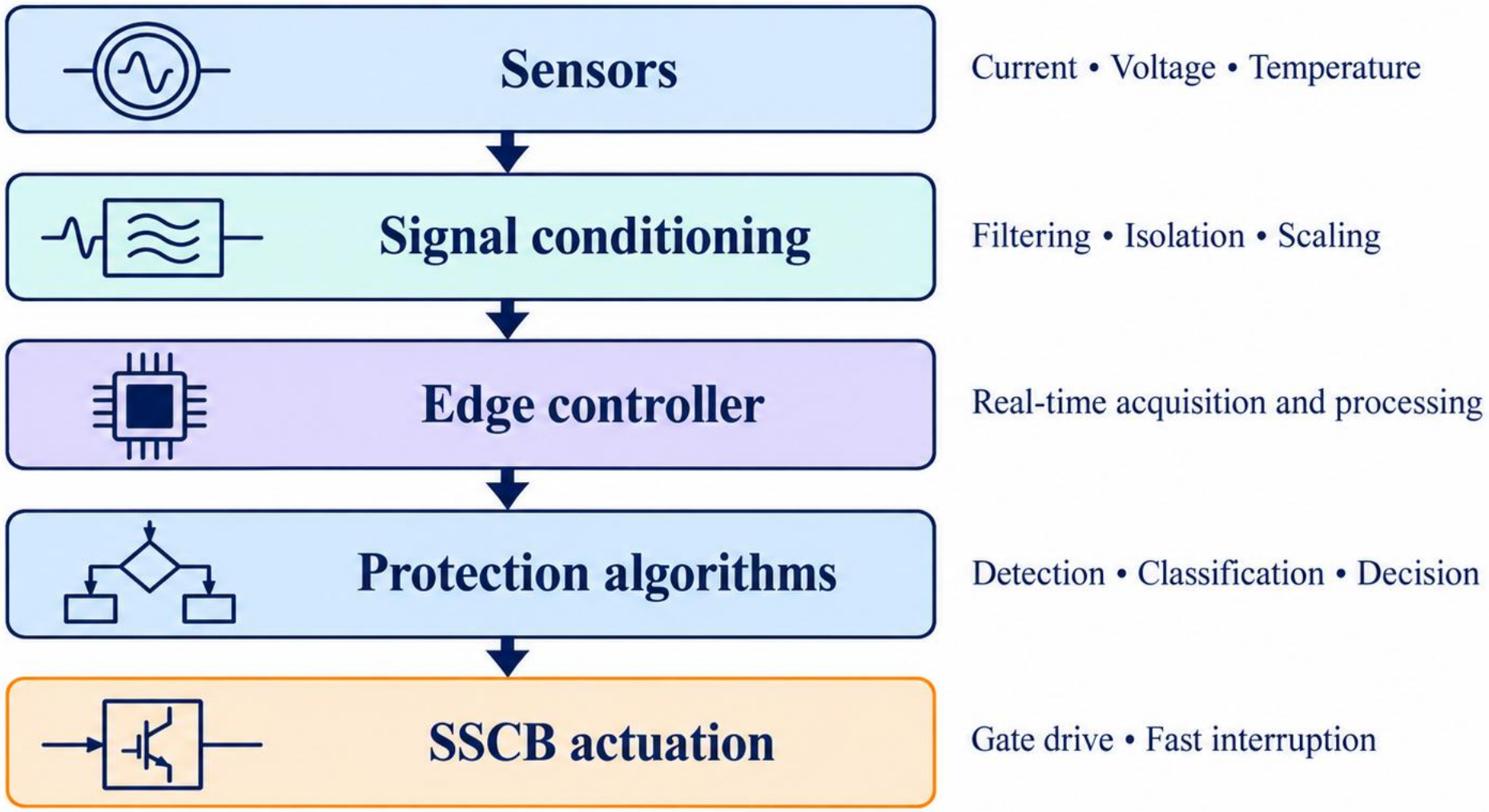
Future approach:
All protection functions embedded in breaker





Solid-state circuit breaker (SSCB)

INTEGRATED PROTECTION ARCHITECTURE

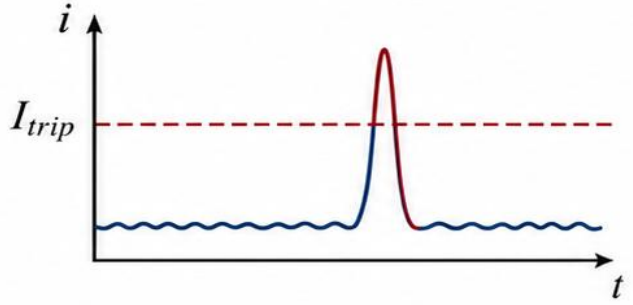


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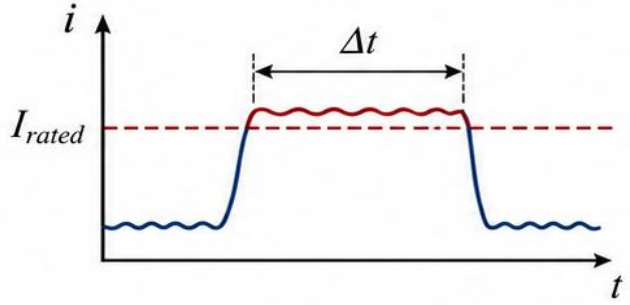
INTEGRATED PROTECTION FUNCTIONS

Overcurrent



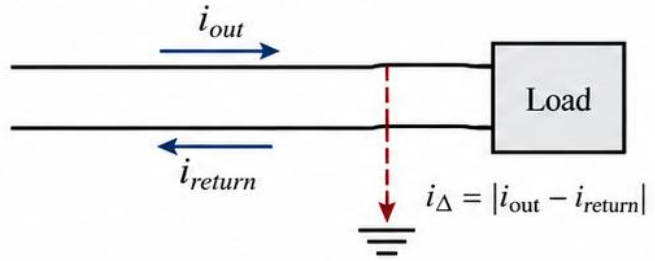
Rapid response to excessive current

Overload



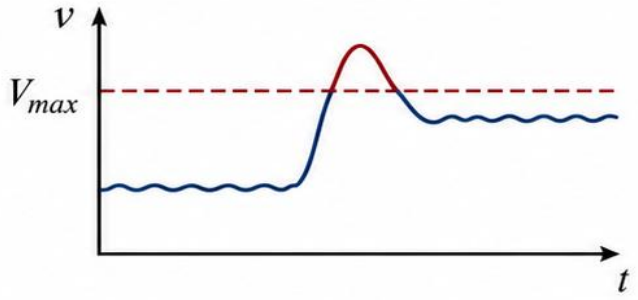
Protection against sustained excessive load

Residual current



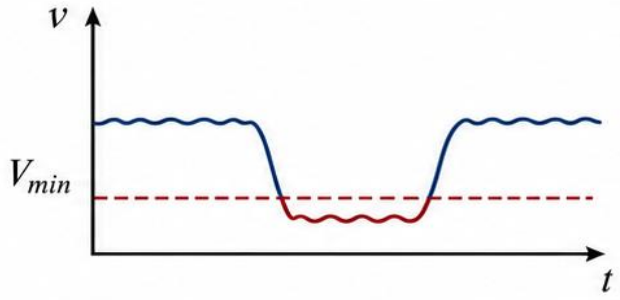
Detect imbalance between outgoing and returning current

Overvoltage



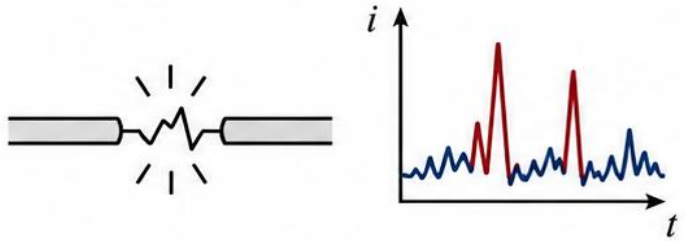
Detect voltage above the permitted limit

Undervoltage



Detect voltage below the permitted limit

Electrical arc



Detect arcing signatures and initiate protection

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DETECTION-TO-INTERRUPTION TIMELINE

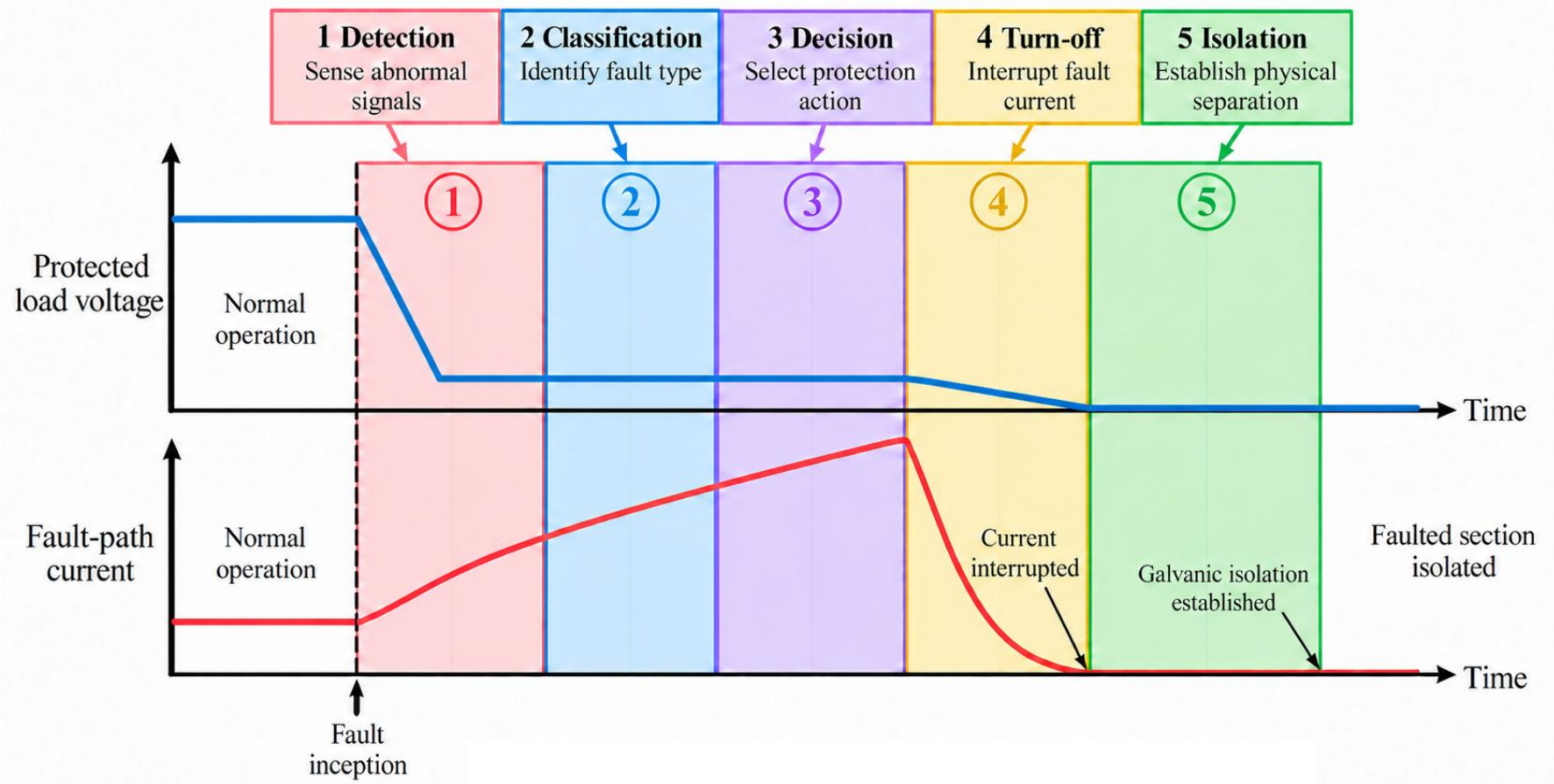
Fault timeline:

- Detection
- Classification
- Decision
- Turn-off
- Isolation

Typical SSCB target:

< 100 µs

(better < 10 µs)



DETECTION-TO-INTERRUPTION TIMELINE

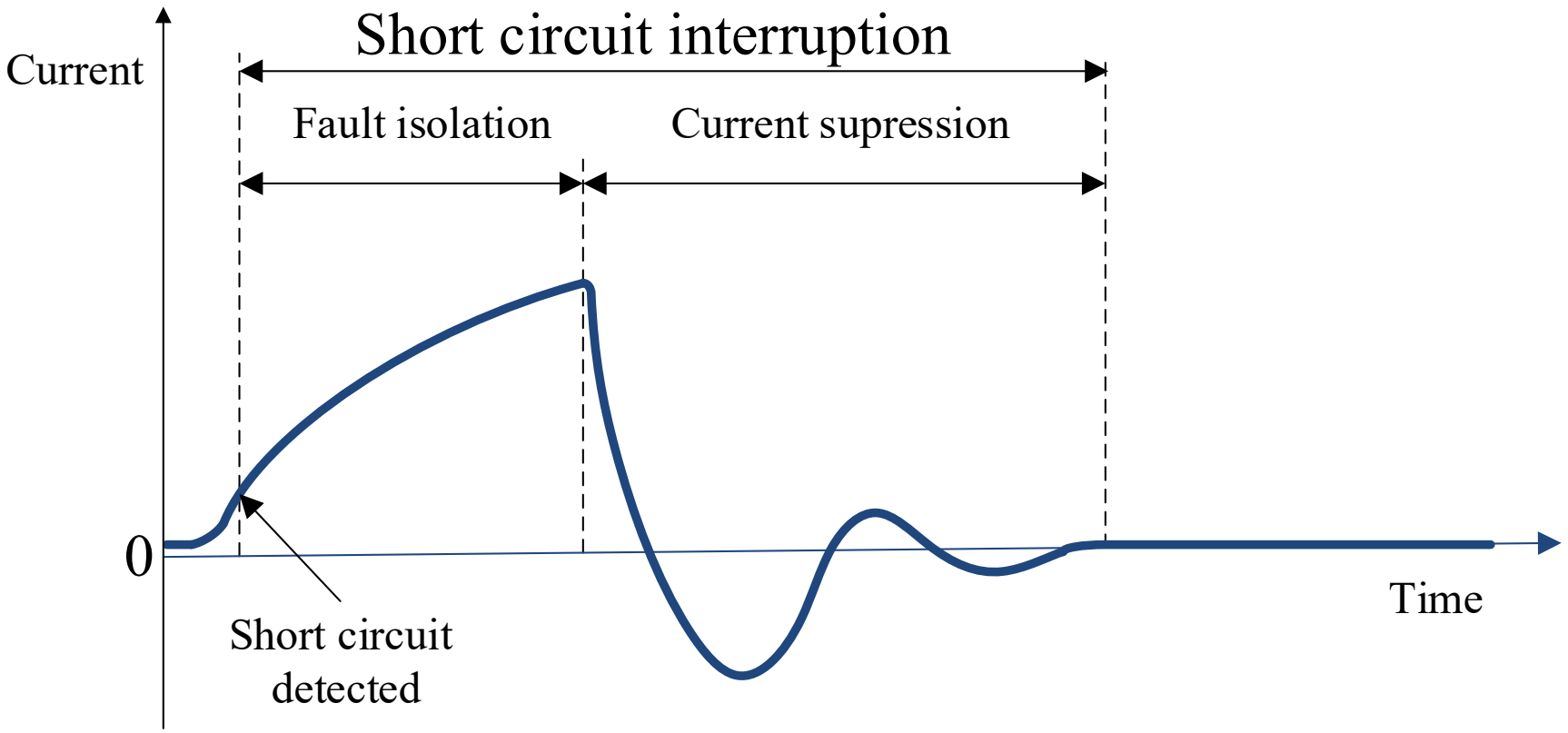
Fault timeline:

- Detection
- Classification
- Decision
- Turn-off
- Isolation

Typical SSCB target:

< 100 μs

(better < 10 μs)



DESIGN



SSCB DESIGN PROCESS

1. Define parameters
2. Estimate fault current
3. Select semiconductor
4. Design sensing
5. Implement protection logic
6. Validate experimentally

SSCB DESIGN PROCESS

1. Define parameters
2. Select semiconductor
3. Design sensing
4. Implement protection logic
5. Validate experimentally

SSCB DESIGN PROCESS (PARAMETERS)

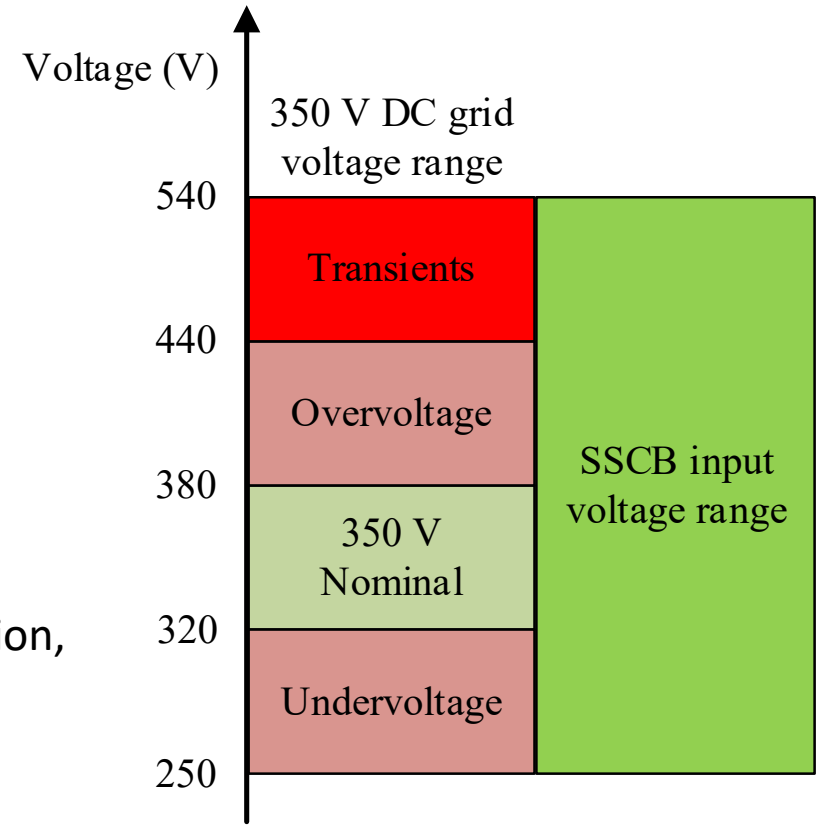
- Some of the parameters are agreed upon:
- voltage level, current limits, control and protection rules.

- Some result from the real topology of the network:
- grid resistance, capacitance, inductance (SC current amplitude and growth rate etc.)

SSCB DESIGN PROCESS (AGREED PARAMETERS)

- Common Voltage levels in residential DC microgrids:
- 12, 24, 48, 350 and 700 V DC
- Control:
- Droop control (or some alternative)
- Typical nominal current values:
- 0…16 A, 24 A, 32 A
- Circuit breaking time:
- < 10 uS

"Current/OS System Public Document 2.1.0" [Online], Current O/S foundation, https://currentos.org/technical-rules/.



Voltage levels in a 350 V DC microgrid

SSCB DESIGN PROCESS (PARAMETERS DEFINED BY GRID TOPOLOGY AND PHYSICAL LAYOUT)

- R_{grid}
- L_{grid}
- C_{grid}
- I_{SC}
- U_p

$$R_{grid} = \rho \times l/A$$

$$L_{grid} = \frac{l\mu_0}{2\pi} cosh^{-1}\left(\frac{S^2 - r_{w1}^2 - r_{w2}^2}{2r_{w1}r_{w1}}\right)$$

$$U_p(t) = L_{grid} \frac{di_{sc}(t)}{dt}$$

- Conductor parameters:
  - physical dimensions (length, radius, distance)
- Assembly parameters:
  - isolation material, permeability
- Devices in grid:
  - input parameters (capacitance, resistance, inductance)

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SSCB DESIGN PROCESS (TYPICAL PARAMETERS DEFINED BY RESIDENTIAL MICROGRID TOPOLOGY AND PHYSICAL LAYOUT)

- Residential microgrid - electrical network of limited dimensions *(one building, vehicle or small district).*

  - $R_{grid} = 6.8\ m\Omega$ *to* $1.37\ \Omega$ *(1 to 200m of wiring)*
  - $L_{grid} = 0.2$ *to* $40\ uH$
  - $C_{grid} =$ *up to several mF (restrictions)*
  - $I_{SC} =$ *tens to hundreds of A (SSCB reaction time)*

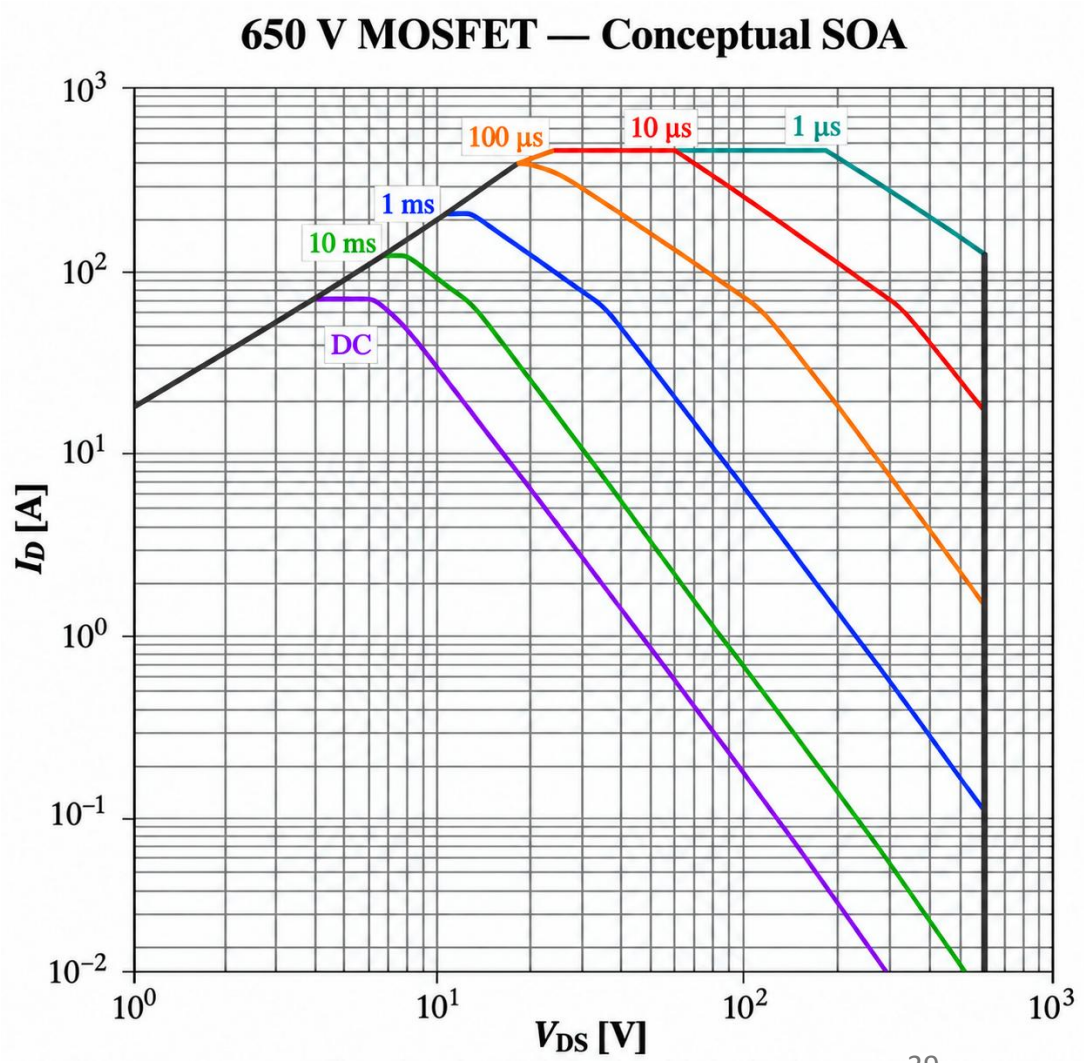
SSCB DESIGN PROCESS

1. Define parameters
2. Select semiconductor
3. Design sensing
4. Implement protection logic
5. Validate experimentally

SSCB DESIGN PROCESS (SEMICONDUCTORS)

Key parameters:

- Blocking Voltage
- Continuous current rating
- Pulsed current and safe operating area
- On-state resistance; voltage — RDS(on); VCE(sat)
- Turn-off time and switching energy
- Transient robustness — *dv/dt*, *di/dt*, avalanche limits

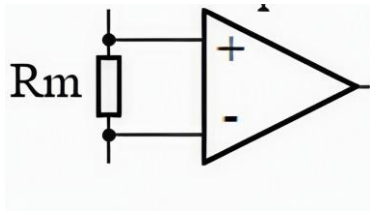


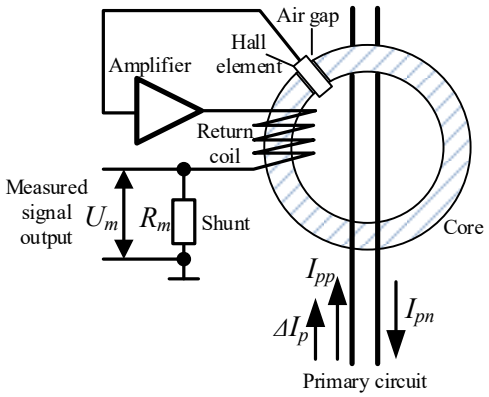
SSCB DESIGN PROCESS

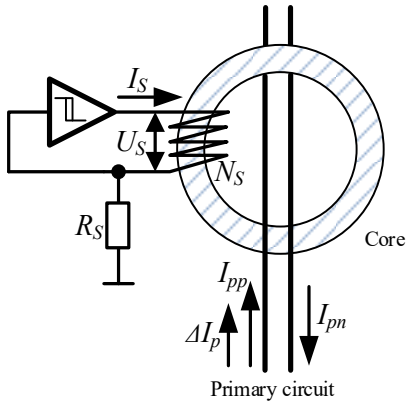
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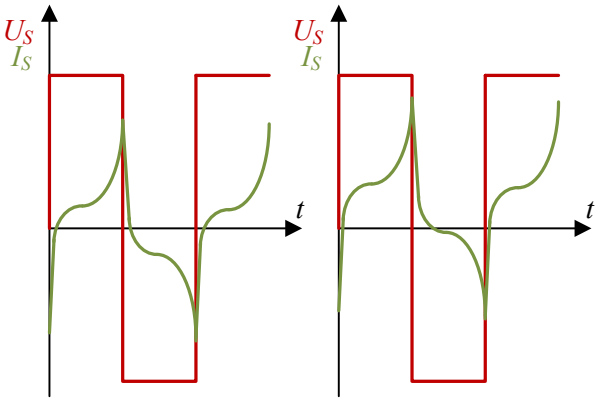
SSCB DESIGN PROCESS (SENSING)

Sensor technology	Suitable for DC	Advantages	Disadvantages
Current transformer	No	Reliability, precizion, galvanic isolation	Saturation of core, dimensions, not suitable for DC
Shunt resistor	Yes	Precizion, cost-effectiveness	Not isolated, Susceptibility to electromagnetic interferences, losses in measurement circuit
Rogowsky coil	No	No saturation effect, compact	Susceptibility to electromagnetic interferences, low preczision
Hall effect	Yes	Precizion, cost-effectiveness, longevity	External magnetic fields lower the precizion, High temperature affects the measurement results
Fluxgate	Yes	Less sensitive to external magnetic fields, high precizion,	Large physical dimensions, high power consumption



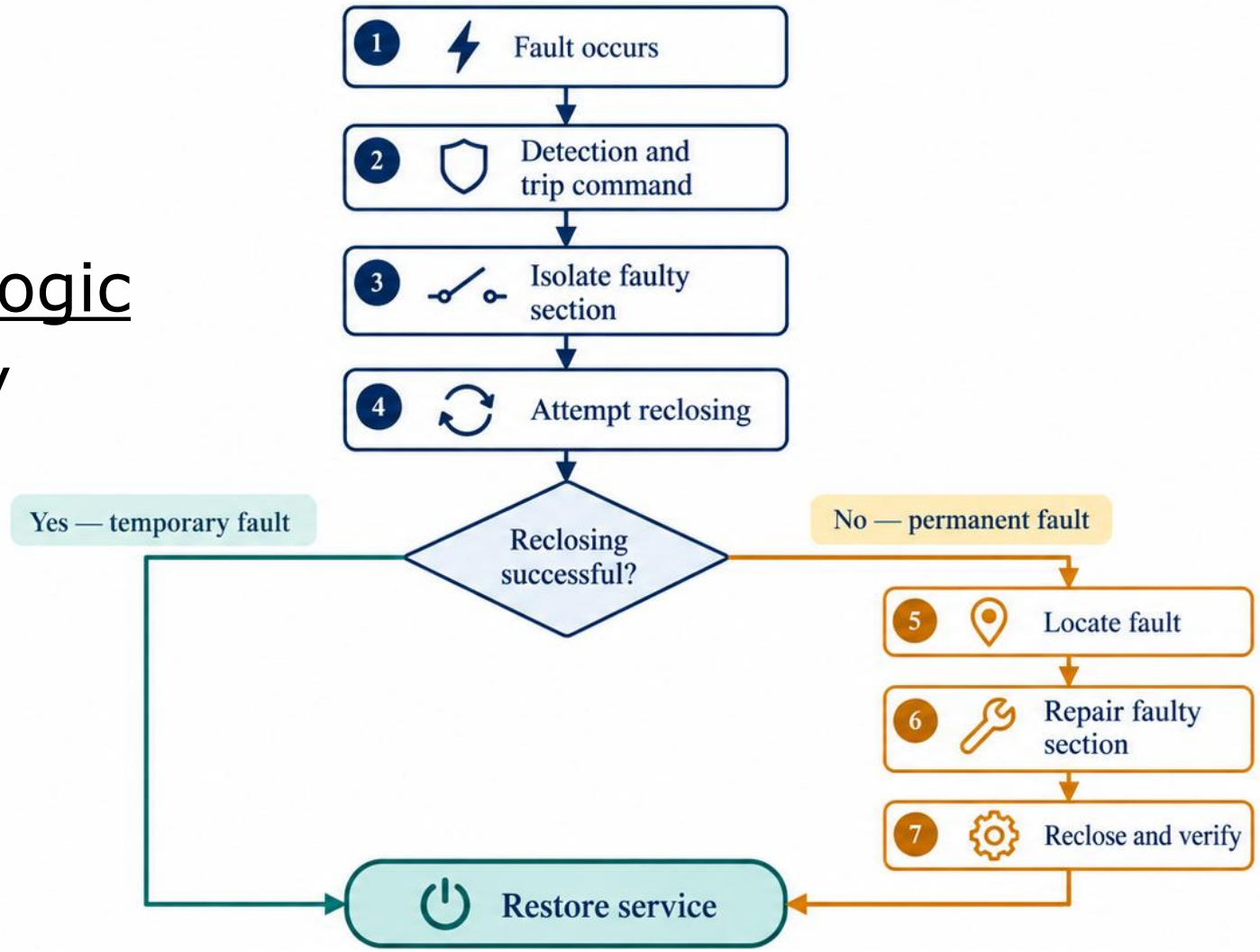






SSCB DESIGN PROCESS (PROTECTION LOGIC)

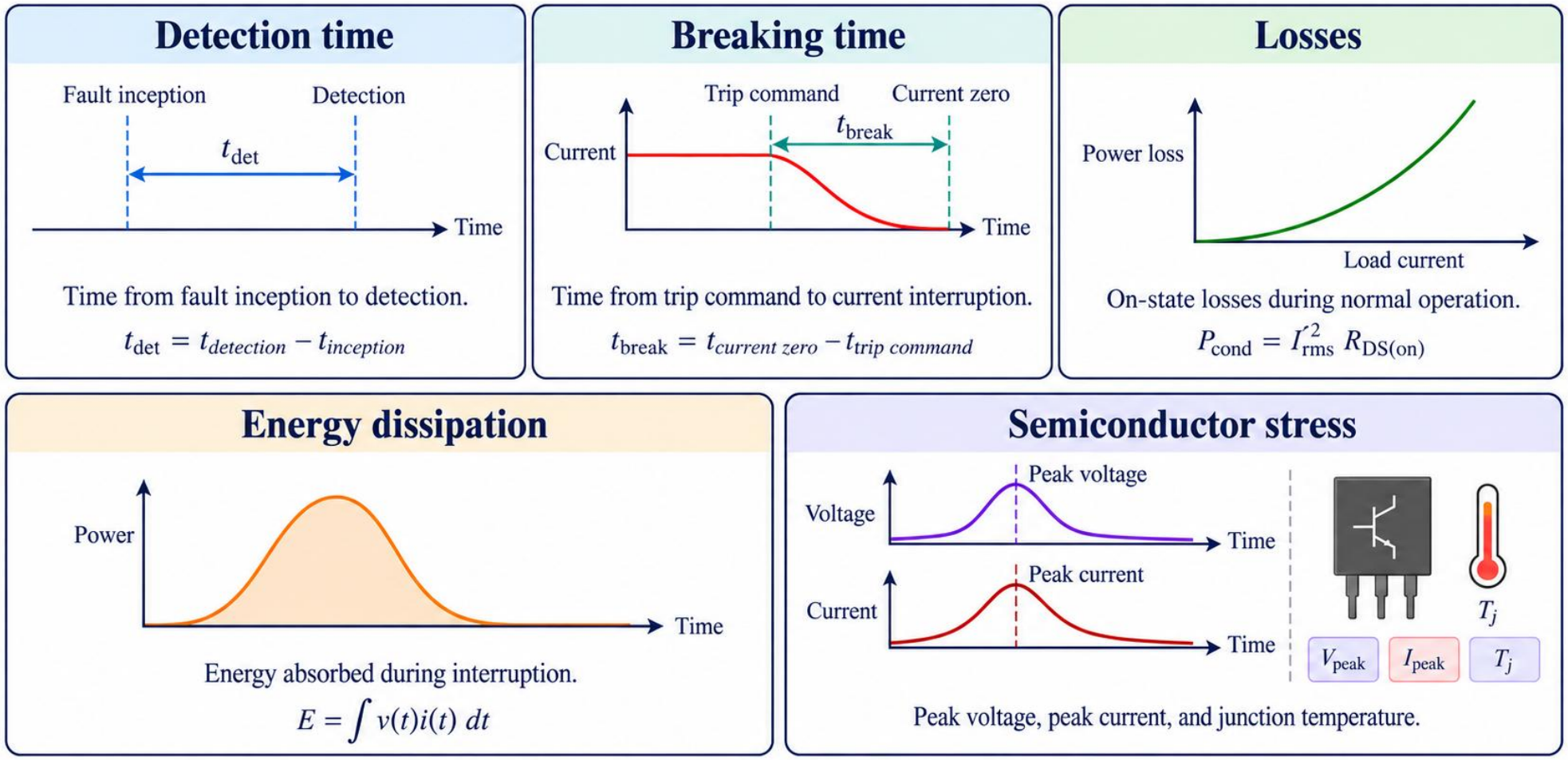
1. Define parameters
2. Select semiconductor
3. Design sensing
4. Implement protection logic
5. Validate experimentally



SSCB DESIGN PROCESS (EXPERIMENTAL VALIDATION)

1. Define parameters
2. Select semiconductor
3. Design sensing
4. Implement protection logic
5. Validate experimentally

SSCB DESIGN PROCESS (EXPERIMENTAL VALIDATION)



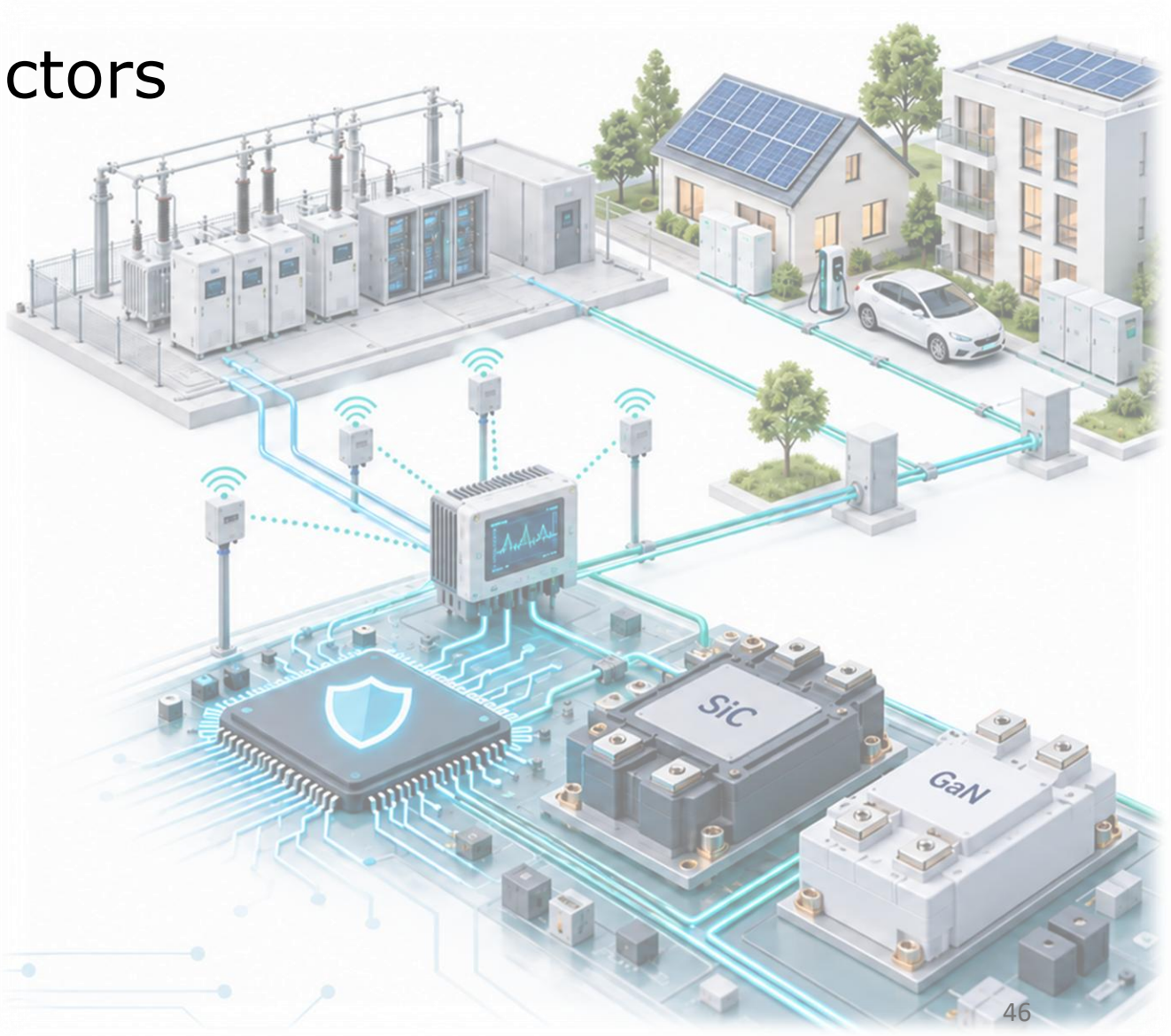
Assess performance under defined fault, voltage, thermal, and circuit conditions.

FUTURE



FUTURE TRENDS

- Wide-bandgap semiconductors
- Protection-on-chip
- Adaptive fault detection
- Digital substations
- DC-ready buildings



RESEARCH OPPORTUNITIES

- Arc fault detection
- Selective coordination
- Cyber-secure protection
- Cost reduction
- Microgrid resilience



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KEY TAKEAWAYS

- Residential DC microgrids are becoming practical
- DC faults are fundamentally different from AC faults.
- Protection remains the major technical challenge.
- SSCBs provide ultrafast interruption.
- Integrated protection creates smarter, safer DC systems.
- Wide-bandgap devices will accelerate adoption.

THANK YOU!

TIME FOR SOME QUESTIONS

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